

CLAIMS

I claim:

1. A method of simultaneously forming at least one capacitor, at least two resistors and at least one metal-oxide semiconductor, comprising the steps of:

providing a structure having an exposed oxide structure; the structure having a capacitor region within at least a portion of the exposed oxide structure; a
5 first resistor region within at least a portion of the exposed oxide structure; a second resistor region within at least a portion of the exposed oxide structure; and a metal-oxide semiconductor region not within at least a portion of the exposed oxide structure;

forming a first polysilicon layer over the structure and the exposed oxide
10 structure;

doping the first polysilicon layer to form a doped first polysilicon layer;

forming an interpoly oxide film over the doped first polysilicon layer;

patterning the interpoly oxide film to form:

a capacitor interpoly oxide film portion within the capacitor region
15 over the oxide structure; and

a second interpoly oxide film portion within the second resistor region over the oxide structure;

forming a second polysilicon layer over the structure;

doping the second polysilicon layer to form a doped second polysilicon
20 layer; and

patterning the doped second polysilicon layer and the doped first polysilicon layer to form:

within the capacitor region: a lower capacitor doped first polysilicon portion underneath at least a portion of the capacitor interpoly oxide film portion, and an overlying upper capacitor second doped polysilicon portion over at least a portion of the patterned capacitor interpoly oxide film portion;

within the first resistor region: a lower first resistor first polysilicon portion and an upper, overlying first resistor second polysilicon portion;

within the second resistor region: a lower second resistor first polysilicon portion underneath at least a portion of the second interpoly oxide film portion; and

within the metal-oxide semiconductor region: a lower metal-oxide semiconductor first polysilicon portion and an overlying metal-oxide semiconductor second polysilicon portion.

2. The method of claim 1, wherein the structure is a substrate and the exposed oxide structure is a field oxide film.

3. The method of claim 1, wherein the structure is a substrate selected from the group consisting of a silicon substrate, a germanium substrate and a gallium arsenide substrate.

4. The method of claim 1, wherein the structure is a silicon substrate.
5. The method of claim 1, wherein the exposed oxide structure has a thickness of from about 4000 to 7500 Å, the first polysilicon layer has a thickness of from about 1000 to 2500 Å, the interpoly film has a thickness of from about 250 to 600 Å, and the second polysilicon layer has a thickness of from about 1000 to 2500 Å.
6. The method of claim 1, wherein the exposed oxide structure has a thickness of from about 4000 to 5500 Å, the first polysilicon layer has a thickness of from about 1500 to 2000 Å, the interpoly film has a thickness of from about 300 to 450 Å, and the second polysilicon layer has a thickness of from about 1500 to 2000 Å.
7. The method of claim 1, wherein the doped first polysilicon layer is doped with a phosphorus dopant or an arsenic dopant; and the doped second polysilicon layer is doped with a phosphorus dopant or an arsenic dopant.
8. The method of claim 1, wherein the doped first polysilicon layer is doped with a phosphorus dopant; and the doped second polysilicon layer is doped with a phosphorus dopant.
9. The method of claim 1, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}16$ to $1\text{E}21$ atoms/cm²; and the doped second

polysilicon layer is doped to a concentration of from about $1\text{E}19$ to $1\text{E}21$ atoms/cm².

10. The method of claim 1, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}18$ to $1\text{E}20$ atoms/cm²; and the doped second polysilicon layer is doped to a concentration of from about $5\text{E}19$ to $5\text{E}20$ atoms/cm².

11. The method of claim 1, wherein one capacitor, two resistors and one metal-oxide semiconductor are formed.

12. A method of simultaneously forming at least one capacitor, at least two resistors and at least one metal-oxide semiconductor, comprising the steps of:

providing a substrate having an exposed oxide structure; the exposed oxide structure being a field oxide film; the substrate having a capacitor region within at least a portion of the exposed oxide structure; a first resistor region within at least a portion of the exposed oxide structure; a second resistor region within at least a portion of the exposed oxide structure; and a metal-oxide semiconductor region not within at least a portion of the exposed oxide structure;

forming a first polysilicon layer over the substrate and the exposed oxide structure;

doping the first polysilicon layer to form a doped first polysilicon layer;

forming an interpoly oxide film over the doped first polysilicon layer;

patterning the interpoly oxide film to form:

15 a capacitor interpoly oxide film portion within the capacitor region
over the oxide structure; and
a second interpoly oxide film portion within the second resistor
region over the oxide structure;
forming a second polysilicon layer over the substrate;
doping the second polysilicon layer to form a doped second polysilicon
20 layer; and
patterning the doped second polysilicon layer and the doped first polysilicon
layer to form:
within the capacitor region: a lower capacitor doped first
polysilicon portion underneath at least a portion of the
25 capacitor interpoly oxide film portion, and an overlying
upper capacitor second doped polysilicon portion over at
least a portion of the patterned capacitor interpoly oxide film
portion;
within the first resistor region: a lower first resistor first polysilicon
30 portion and an upper, overlying first resistor second
polysilicon portion;
within the second resistor region: a lower second resistor first
polysilicon portion underneath at least a portion of the
second interpoly oxide film portion; and
35 within the metal-oxide semiconductor region: a lower metal-oxide
semiconductor first polysilicon portion and an overlying
metal-oxide semiconductor second polysilicon portion.

13. The method of claim 12, wherein the substrate is a silicon substrate, a germanium substrate or a gallium arsenide substrate.

14. The method of claim 12, wherein the substrate is a silicon substrate.

15. The method of claim 12, wherein the exposed oxide structure has a thickness of from about 4000 to 7500 Å, the first polysilicon layer has a thickness of from about 1000 to 2500 Å, the interpoly film has a thickness of from about 250 to 600 Å, and the second polysilicon layer has a thickness of from about 1000 to 2500 Å.

16. The method of claim 12, wherein the exposed oxide structure has a thickness of from about 4000 to 5500 Å, the first polysilicon layer has a thickness of from about 1500 to 2000 Å, the interpoly film has a thickness of from about 300 to 450 Å, and the second polysilicon layer has a thickness of from about 1500 to 2000 Å.

17. The method of claim 12, wherein the doped first polysilicon layer is doped with a phosphorus dopant or an arsenic dopant; and the doped second polysilicon layer is doped with a phosphorus dopant or an arsenic dopant.

18. The method of claim 12, wherein the doped first polysilicon layer is doped with a phosphorus dopant; and the doped second polysilicon layer is doped with a phosphorus dopant.

19. The method of claim 12, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}16$ to $1\text{E}21$ atoms/cm²; and the doped second polysilicon layer is doped to a concentration of from about $1\text{E}19$ to $1\text{E}21$ atoms/cm².

20. The method of claim 12, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}18$ to $1\text{E}20$ atoms/cm²; and the doped second polysilicon layer is doped to a concentration of from about $5\text{E}19$ to $5\text{E}20$ atoms/cm².

21. The method of claim 12, wherein one capacitor, two resistors and one metal-oxide semiconductor are formed.

22. A method of simultaneously forming at least one capacitor, at least two resistors and at least one metal-oxide semiconductor, comprising the steps of:

providing a structure having an exposed oxide structure having a thickness of from about 4000 to 7500 Å; the structure having a capacitor region within at least a portion of the exposed oxide structure; a first resistor region within at least a portion of the exposed oxide structure; a second resistor region within at least a portion of the exposed oxide structure; and a metal-oxide semiconductor region not within at least a portion of the exposed oxide structure;

forming a first polysilicon layer over the structure and the exposed oxide structure; the first polysilicon layer having a thickness of from about 1000 to 2500 Å;

doping the first polysilicon layer to form a doped first polysilicon layer;

forming an interpoly oxide film over the doped first polysilicon layer; the interpoly film having a thickness of from about 250 to 600Å;

patterning the interpoly oxide film to form:

15 a capacitor interpoly oxide film portion within the capacitor region over the oxide structure; and

 a second interpoly oxide film portion within the second resistor region over the oxide structure;

 forming a second polysilicon layer over the structure; the second polysilicon
20 layer having a thickness of from about 1000 to 2500Å;

 doping the second polysilicon layer to form a doped second polysilicon layer; and

 patterning the doped second polysilicon layer and the doped first polysilicon layer to form:

25 within the capacitor region: a lower capacitor doped first polysilicon portion underneath at least a portion of the capacitor interpoly oxide film portion, and an overlying upper capacitor second doped polysilicon portion over at least a portion of the patterned capacitor interpoly oxide film
30 portion;

 within the first resistor region: a lower first resistor first polysilicon portion and an upper, overlying first resistor second polysilicon portion;

35 within the second resistor region: a lower second resistor first
 polysilicon portion underneath at least a portion of the
 second interpoly oxide film portion; and
 within the metal-oxide semiconductor region: a lower metal-oxide
 semiconductor first polysilicon portion and an overlying
 metal-oxide semiconductor second polysilicon portion.

23. The method of claim 22, wherein the structure is a substrate and the exposed oxide structure is a field oxide film.

24. The method of claim 22, wherein the structure is a substrate selected from the group consisting of a silicon substrate, a germanium substrate and a gallium arsenide substrate.

25. The method of claim 22, wherein the structure is a silicon substrate.

26. The method of claim 22, wherein the exposed oxide structure has, , , and the.

27. The method of claim 22, wherein the exposed oxide structure has a thickness of from about 4000 to 5500Å, the first polysilicon layer has a thickness of from about 1500 to 2000Å, the interpoly film has a thickness of from about 300 to 450Å, and the second polysilicon layer has a thickness of from about 1500 to 2000Å.

28. The method of claim 22, wherein the doped first polysilicon layer is doped with a phosphorus dopant or an arsenic dopant; and the doped second polysilicon layer is doped with a phosphorus dopant or an arsenic dopant.

29. The method of claim 22, wherein the doped first polysilicon layer is doped with a phosphorus dopant; and the doped second polysilicon layer is doped with a phosphorus dopant.

30. The method of claim 22, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}16$ to $1\text{E}21$ atoms/cm²; and the doped second polysilicon layer is doped to a concentration of from about $1\text{E}19$ to $1\text{E}21$ atoms/cm².

31. The method of claim 22, wherein the doped first polysilicon layer is doped to a concentration of from about $1\text{E}18$ to $1\text{E}20$ atoms/cm²; and the doped second polysilicon layer is doped to a concentration of from about $5\text{E}19$ to $5\text{E}20$ atoms/cm².

32. The method of claim 22, wherein one capacitor, two resistors and one metal-oxide semiconductor are formed.